Odd Order MESFET Multipliers with Broadband, Efficient, Low Spurious Response

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ABSTRACT

A novel circuit structure for odd order MESFET frequency multipliers has been developed using a generalized design approach. Improvements in efficiency, bandwidth and spurious harmonic rejection have been achieved via accurate models under large signal conditions.

INTRODUCTION

In the past, numerous papers have been written identifying the advantages of using active multipliers over passive multipliers at frequencies above 2 GHz [1,2]. The key features of the active multipliers superior performance are: low power operation, wide bandwidth, good harmonic rejection, efficient, good isolation, low distortion, small, and temperature stable. To date, only low order MESFET frequency multipliers have been presented [3]. Although the need for developing this design approach has been recognized, there has been a void in defining design and performance characteristics of higher order frequency multiplication.

A novel solution to this problem is to develop a general design approach which is applicable to higher order frequency multiplications. This approach will be applied to the design of a X3 and X5 active MESFET multiplier. A key element to this design is the elimination of the traditional idler circuit which limits bandwidth [4,7]. This is replaced with matching structures that provide a good match to wanted harmonics while providing a mismatch to unwanted harmonics. The designs of this paper display superior efficiency (greater than 10*log[1/N]) across a broadband with low AM-to-PM conversion noise and excellent spurious suppression.

DESIGN APPROACH

The design approach consists of three main steps: nonlinear device characterization, input match for gain, and output match for harmonic selection and enhancement. A large signal model for the device (GaAs MESFET, NE67483) was extracted to be used on the HP® MDS® design platform. After obtaining an accurate large signal model, the device was simulated for optimum bias conditions including Vds, Vgs and RF input power to obtain the desired harmonic response. In a parallel effort the device was aligned in the lab for optimum bias conditions Vds, Vgs and RF input power to obtain the desired harmonic response. Once the correlation between the simulated and measured response is achieved, the design can proceed with a high level of confidence. The gate to source capacitance versus voltage is modeled by taking advantage of the nonlinear characteristics of the MESFET which can be viewed as a diode. The input circuit of the FET acts as a nonlinear element generating harmonics with an input driving signal of appropriate power. There are two different bias conditions which support harmonic generation[6]:

1) At Idss (Vgs=0) where the input signal drives the gate diode into forward conduction,
2) At Pinch-off voltage (Ids=0) where the gate voltage swings below pinch-off to create a current clipping effect.

With the bias conditions and input power level established, the device was aligned with triple stub tuners at the input and output (load pull measurements[5]) to establish measured data of optimum input and output matching circuit. These measured large signal S-parameters showed close correlation with the large signal computer model.

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The input circuit was designed to provide low VSWR while maintaining a match for high gain at the desired harmonic. This included generating a circuit file using the large signal model and generating S11 measurements under large signal conditions. Comparing the S11 measured response of the input triple stub tuners indicated that the optimum input matching circuit correspond to the conjugate match of S11 of the simulation under large signal conditions. The input circuit also includes a 1/4 λ open stub at the C band output frequency (3fo) to provide an RF short for any leakage of the output frequency at the input.

The output circuit was designed to enhance the desired harmonic while maintaining rejection of unwanted harmonics. This included generating a circuit file using the large signal model and generating S22 measurement under large signal conditions. In order to maintain the device under large signal conditions a large signal was provided to drive the input port while a small RF signal at a small offset frequency was injected at the output port and the reflected signal measured via an ideal detector. Comparing the S22 measured response of the output triple stub tuners indicated that the optimum output matching circuit corresponds to the conjugate match of S22 of the simulation under large signal conditions. The output circuit also included 1/4λ at 4fo and at 6fo open stubs. Since the fundamental tone (fo) can not be eliminated using RF short for an odd integer multiplier, a bandpass filter was added the output. For the C band X3 multiplier an initerdigital microstrip configuration was added. A parallel edged coupled microstrip filter was added to the X5 multiplier. These filters provided the desired rejection at the fundamental and spurious without sacrificing high performance at the desired harmonic.

RESULTS

The active device (NE76483 was chosen for space application) was modeled via measurements of s-parameters and current-voltage in the IV plane. A detailed model was developed for use in HP® MDS®.

The X3 C band active MESFET multiplier exhibits close correlation between measured and modeled results:

	Simulated	Measured
Input Freq.	2 GHz	2 GHz
Output Freq.	6 GHz	6 GHz
1dB BW	15 %	17 %
Input Power	+6 dBm	+6 dBm
Output Power	+1.5 dBm	+2.44 dBm
Conversion Gain	-3.8 dB	-2.64 dB
Filter Loss	0.7 dB	0.92 dB
Bias Condition	Idss	Idss
Harmonic Rejection	25 dBc	30 dBc

Figure 1 shows the actual MIC assembly including multiplier/filter. Figures 2,3 and 4 show the measured electrical performance of the X3 multiplier.

The X5 X-band active MESFET multiplier shows close agreement between measured and modeled results:

	Simulated	Measured
Input Freq.	2 GHz	2 GHz
Output Freq.	10 GHz	10 GHz
Input Power	+11 dBm	+12 dBm
Output Power	+2.0 dBm	+5.3 dBm
Conversion Gain	-9.0 dB	-6.7 dB
Bias Condition	Vpinchoff	Vpinchoff
Harmonic Rejection	25 dBc	35 dBc

The spectral performance of the X5 multiplier is shown on Figure 5 and 6.

CONCLUSION

A design methodology was presented to achieve maximum efficiency for higher order multipliers. With careful verification of a large signal model of the active device (MESFET, PHEMT) and correlating load pull measurements with initial simulations lays the foundation for a design of high order multiplication with minimal variation of simulated vs. measured results. Carefully designing the input and output circuitry to incorporate filtering which provide the proper load at the unwanted harmonics for maximum rejection and minimize leakage at the input will result with maximum efficiency, bandwidth, and improved AM/PM. This is possible in spite of the fact the no idler circuit was used.

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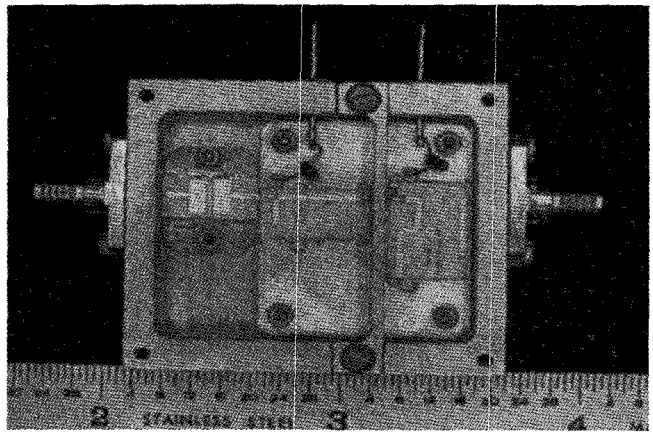

Figure 1: C Band X3 Active Multiplier Assembly

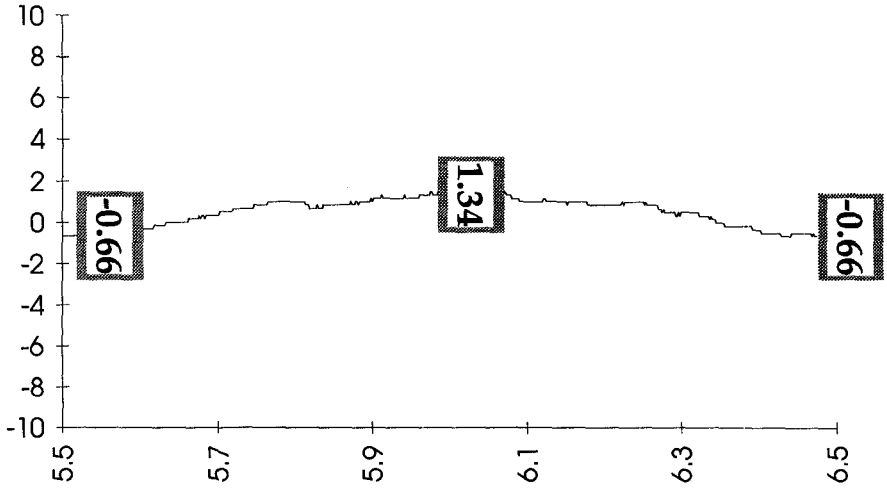

Figure 2: C Band X3 Active Multiplier Broadband Response

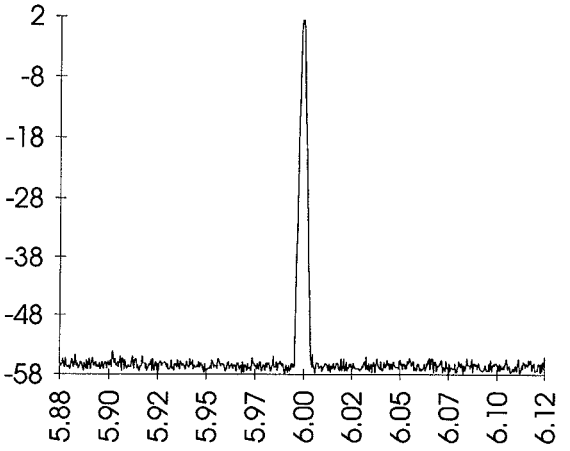

Figure 3: C Band X3 Active Multiplier output response @ 6 GHz

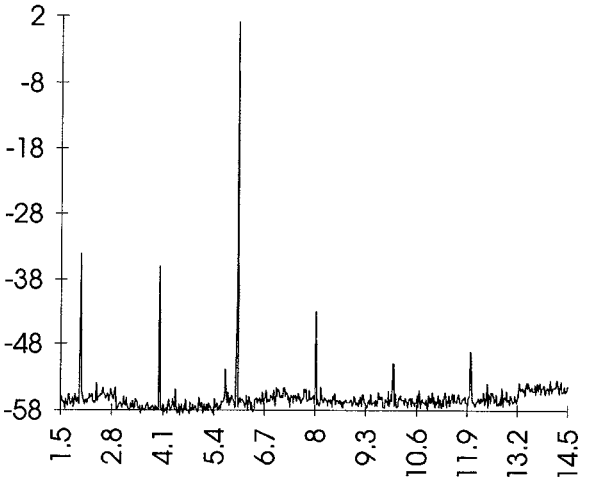

Figure 4: C Band X3 Active Multiplier Output Harmonic Response

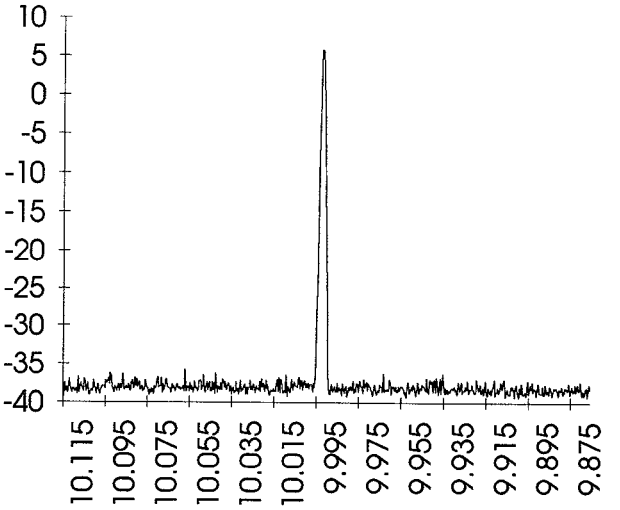

Figure 5: X Band X5 Active Multiplier output response @ 10 GHz

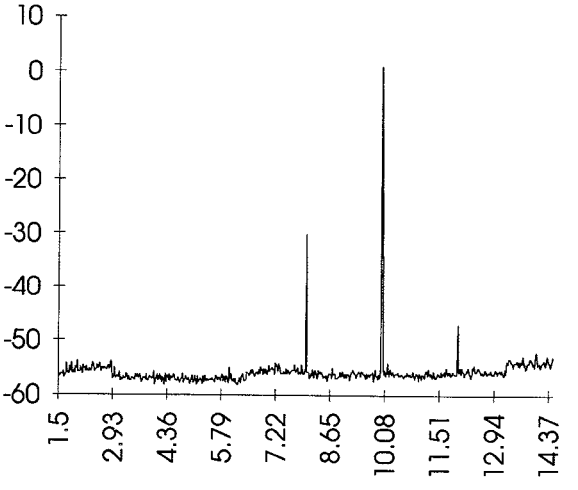

Figure 6: X Band X5 Active Multiplier Output Harmonic Response